

WPT6035DDA Datasheet

Wireless Power Receiver Controller

Description

The WPT6035DDA is 3.5A receiver controller with wide input voltage. The highly integrated chip design enables it to achieve high power density, and special power processing mode assists the controller on achieving high efficiency at light load or standby condition. Provides over current protection, thermal shutdown protection. The device is available in an ESOP-8 package.

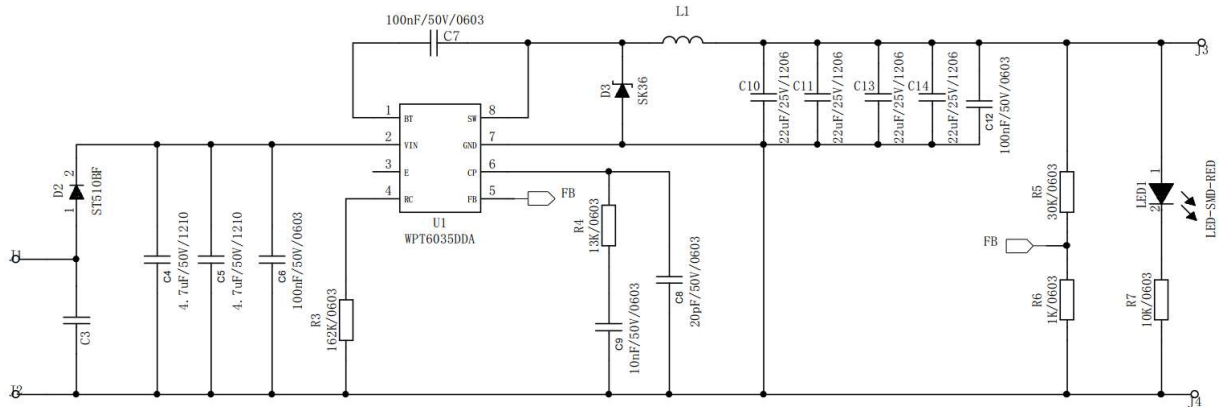
Features

- Compatible With Transmitter Wide Voltage Input.
- 3.5A Continuous Output Current.
- Over- Current and Over-Temperature Protection.
- Lower Energy Pickup Threshold.
- Achieve High Power Density Design.

Applications

- Industrial and Consumer Electronics.
- High Protection Occasions.
- High Speed Rotating Occasion.
- Isolated Power Supply.
- Wireless Induction Heating

Typical Application



ABSOLUTE MAXIMUM RATINGS

DESCRIPTION	MIN	MAX	UNIT
Out voltage	1.2	48	V
output current	0	3000	mA
Operating junction temperature TJ	-40	+150	°C
Storage temperature TSTG	-65	+150	°C

Example

Mature cases: WP3025T-D50&WP2425R-D50 used WPT6035DDA

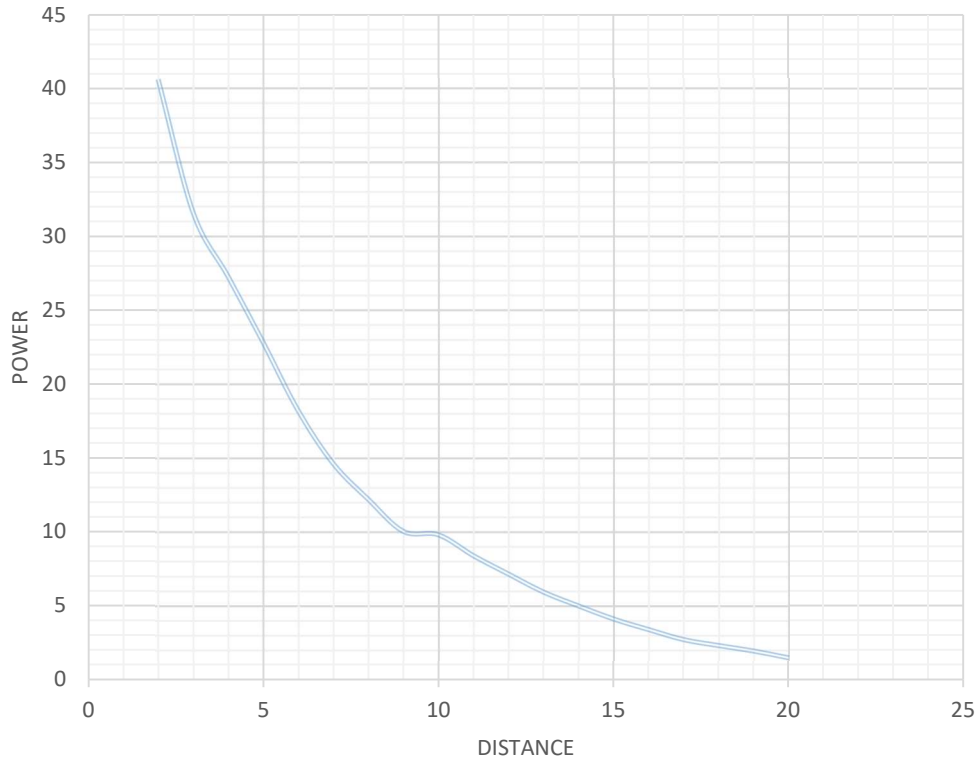


Figure 1. Maximum Output Power vs Coil Distance

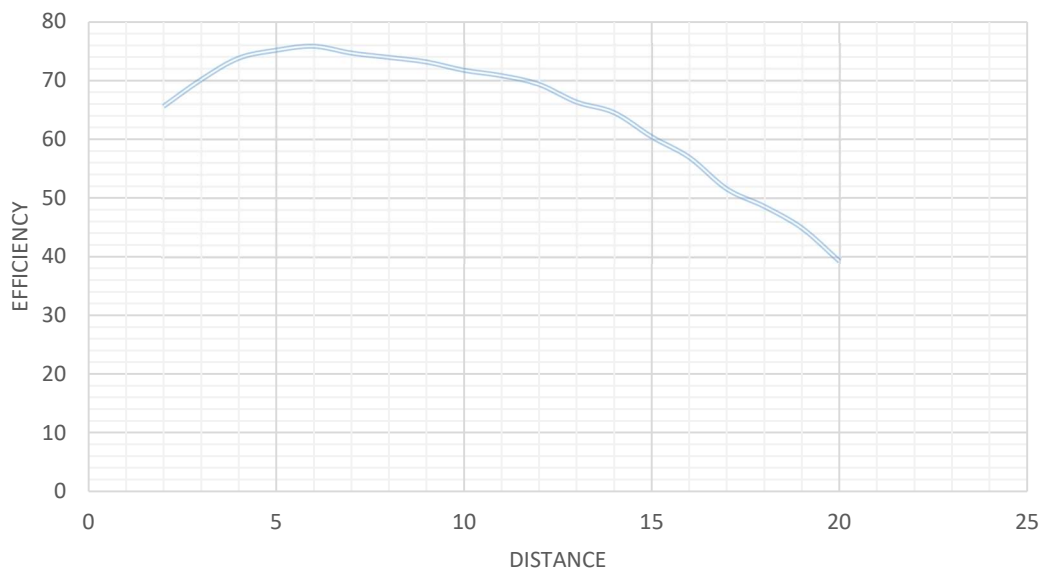
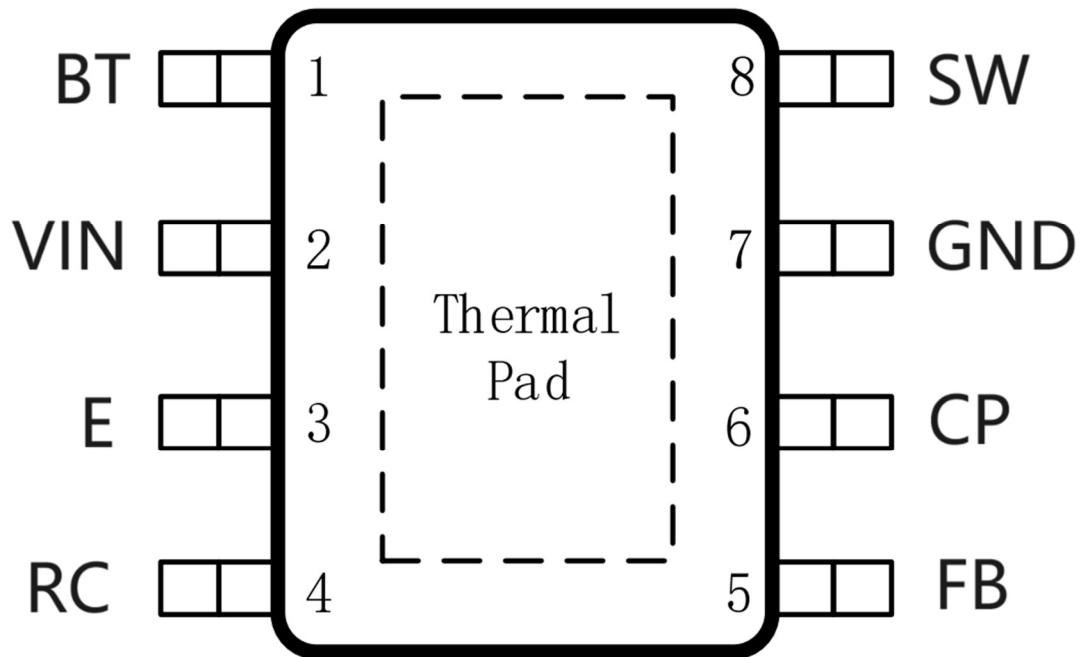


Figure 2. Efficiency at Maximum Power vs Coil Distance

PIN CONFIGURATION



PIN FUNCTIONS

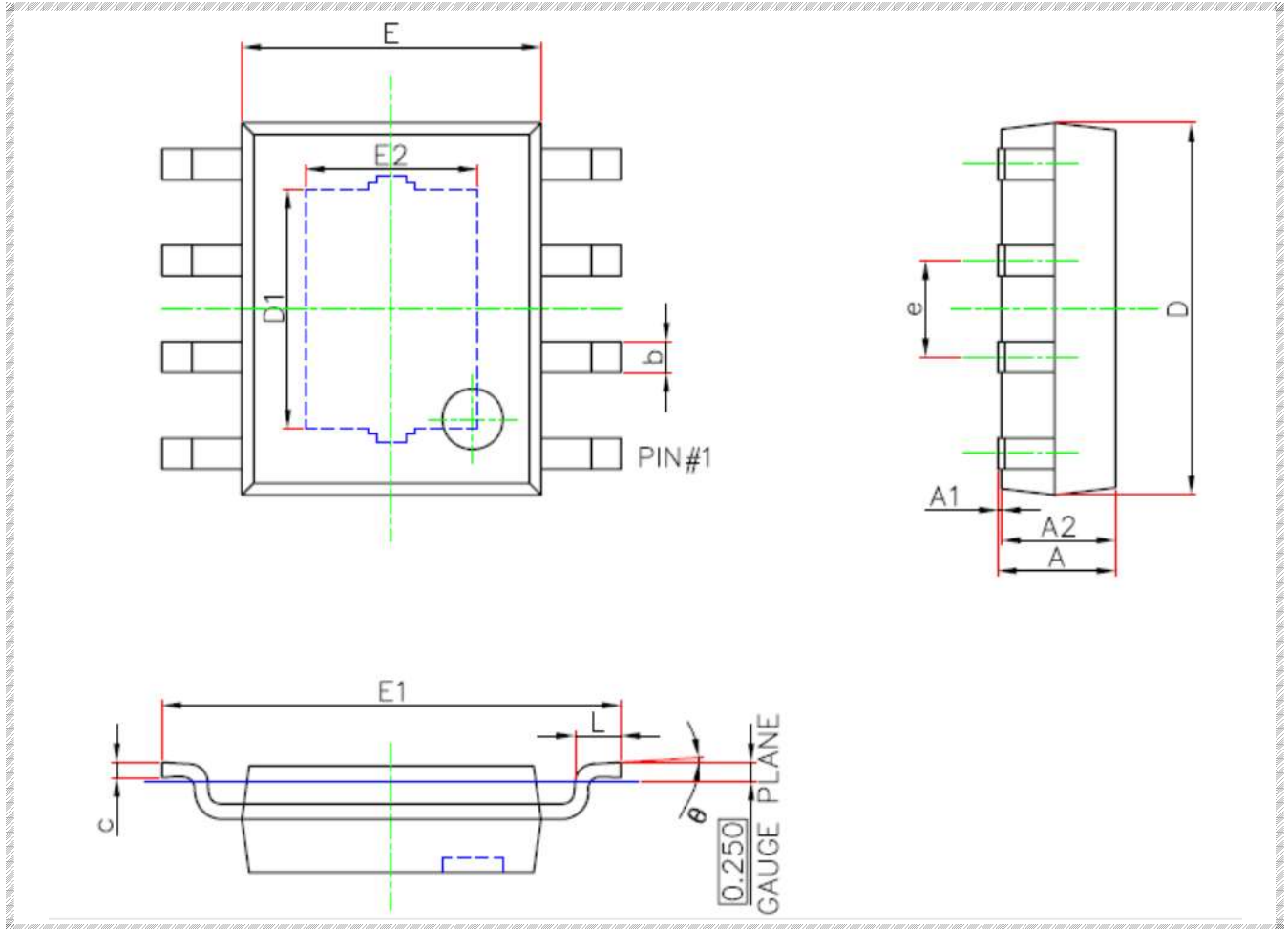
NAME	NO.	PIN FUNCTION
BT	1	Power supply for internal power device drive
VIN	2	Input supply voltage
E	3	Enable pin, Pull below to disable the controller
RC	4	Basic frequency setting
FB	5	The tap of external feedback resistor sets the output voltage
CP	6	Connect to frequency loop compensation network
GND	7	Ground
SW	8	Switching output

DEVICE ORDER INFORMATION

PART NUMBER	PACKAGE MARKING	PACKAGE DISCRIPTION
WPT6035DDA	WPT6035DDA YYWW	ESOP-8

Package Information

ESOP8



Unit:mm

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min.	Max.	Min.	Max.
A	1.300	1.700	0.051	0.067
A1	0.000	0.100	0.000	0.004
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
D1	3.050	3.250	0.120	0.128
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
E2	2.160	2.360	0.085	0.093
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

1. All linear dimensions are in millimeters.
2. Thermal pad shall be soldered on the board.

Layout Guideline

Proper PCB layout is a critical for WPT6035DDA's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Power grounding scheme is very critical because of carrying power, thermal, and glitch/bouncing noise associated with clock frequency. The thumb of rule is to make ground trace lowest impedance and power are distributed evenly on PCB. Sufficiently placing ground area will optimize thermal and not causing over heat area.
2. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
3. Output side diode should be place as close to SW pin and the ground as possible to reduce parasitic effect.
4. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impedance of grounding.
5. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. The power pad should be connected to bottom PCB ground planes using multiple vias directly under the IC.

The center thermal pad should always be soldered to the board for mechanical strength and reliability, using multiple thermal vias underneath the thermal pad. Improper soldering thermal pad to ground plate on PCB will cause SW higher ringing and overshoot besides downgrading thermal performance. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.

6. Output inductor and diode should be placed close to the SW pin. The switching area of the PCB conductor minimized to prevent excessive capacitive coupling.

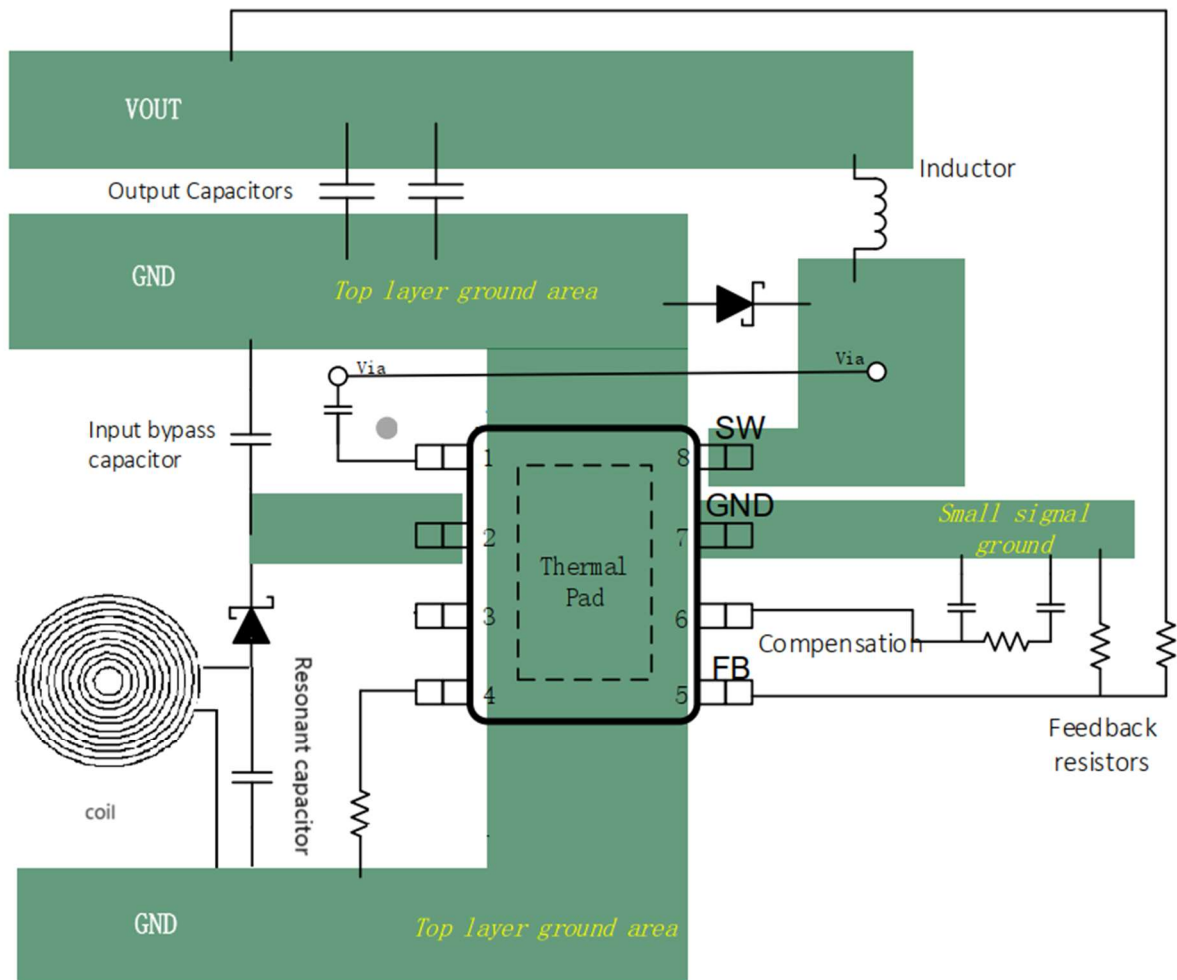
7. The RC terminal is sensitive to noise so the RT resistor should be located as close as possible to the IC and routed with minimal lengths of trace.

8. RT resistors and feedback components should connect to small signal ground which must return to the GND pin without any interleaving with power ground.

9. Route BT capacitor trace on the other layer than top layer to provide wide path for topside ground.

10. For achieving better thermal performance, a four-layer layout is strongly recommended Layout.

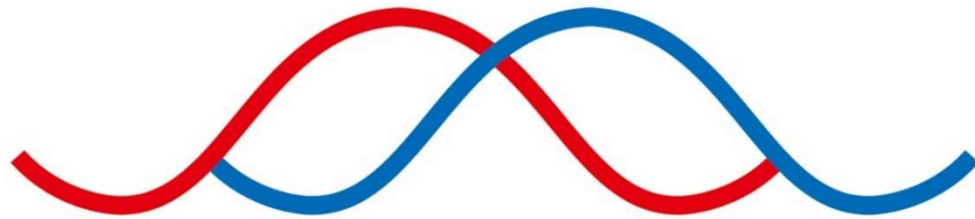
Examples



Revision History

The following table shows the revision history for this document.

Date	Version	Content	Author
2021.03.10	1.0.0	1. New	Chumy



W I R E L E S S P O W E R

Shenzhen WUPAI Technology Co., Ltd.

WIRELESSPOWER.CN